

# ITER Fast Plant System Controller Prototype Based on PXI Platform

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on behalf of CIEMAT/UPM/IST/ITER team

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IPFN, Instituto Superior Técnico

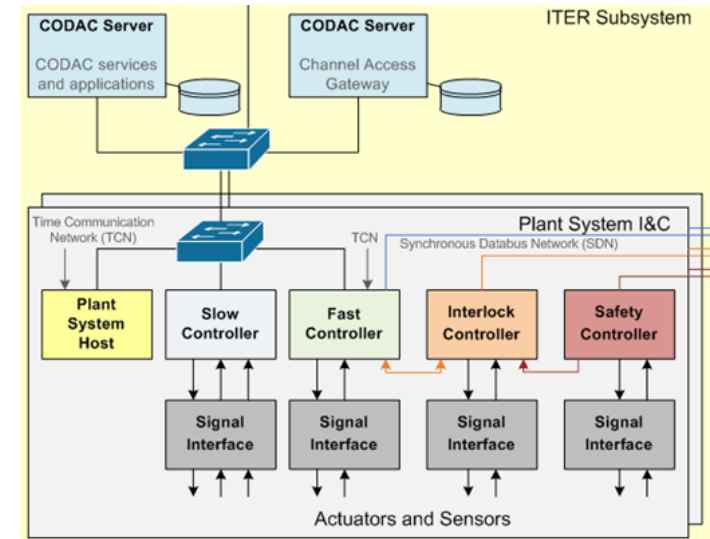
ITER Organization



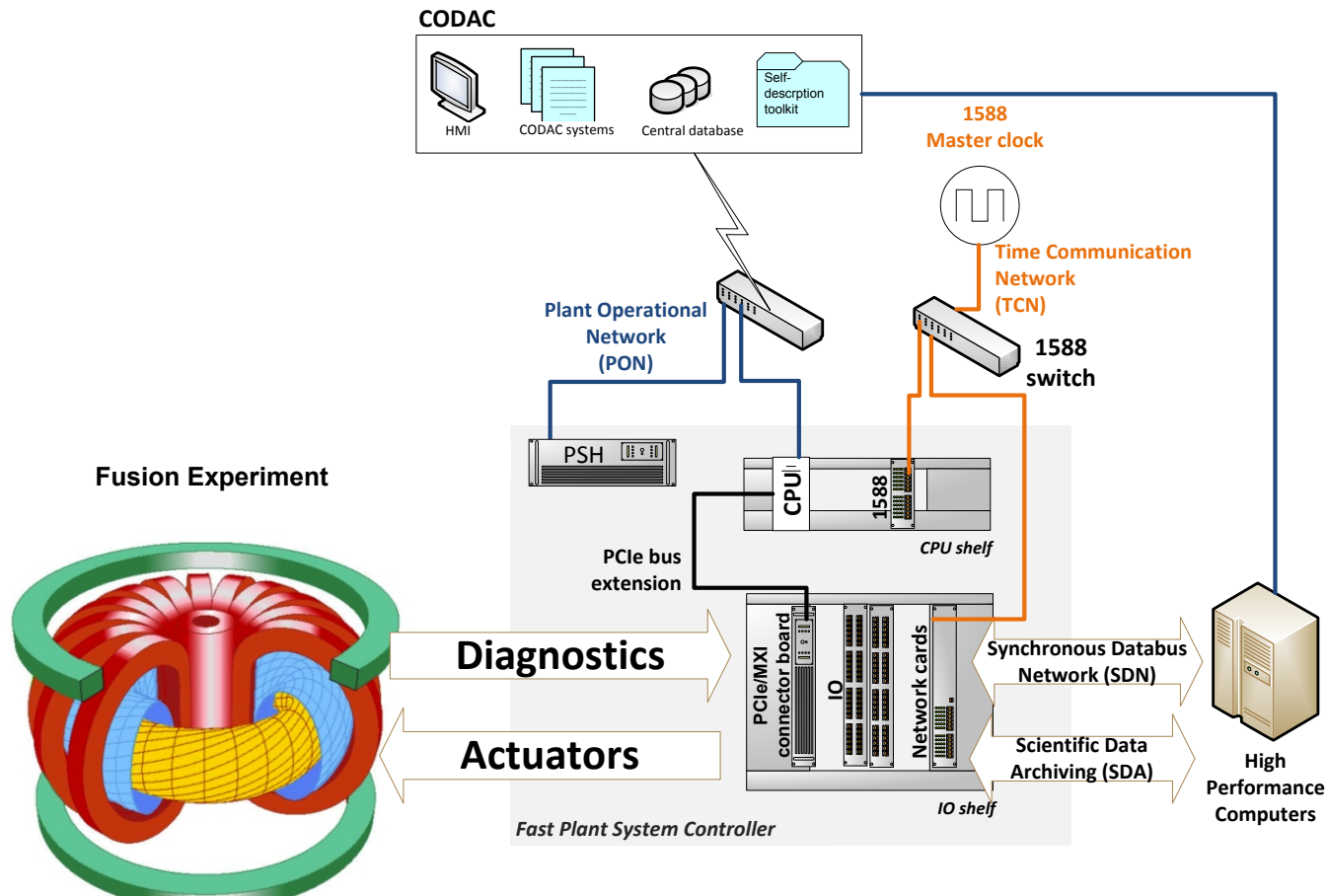
- Project scope and requirements.
- FPSC HW elements.
- FPSC SW elements.
  - Applications running in the controller.
  - Data acquisition. FPSC control using EPICS PVs
  - Streaming/archiving applications
- Conclusions.

# Project Scope and requirements

- ITER CODAC Design identifies two types of Plant System Controllers (PSC):
  - Slow PSC is based on industrial automation technology(control loops rates <1 kHz).
  - The Fast PSC is based on embedded technology with higher sampling rates and more stringent real-time requirements.
- Essentials requirements of FPSC:
  - Data acquisition and preprocessing
  - Interfacing with the networks (PON, TCN, SDN, streaming/archiving networks)
  - LINUX OS and EPICS IOC. System setup and operation using process variables.
  - COTS solutions.
- **Developing a prototype FPSC targeting Data Acquisition for ITER IO**
  - Two different form factors for the implementation:
    - ATCA based solution (IST)
    - PCIe based solution (CIEMAT/UPM)
  - A two steps approach: Alpha and Beta version.

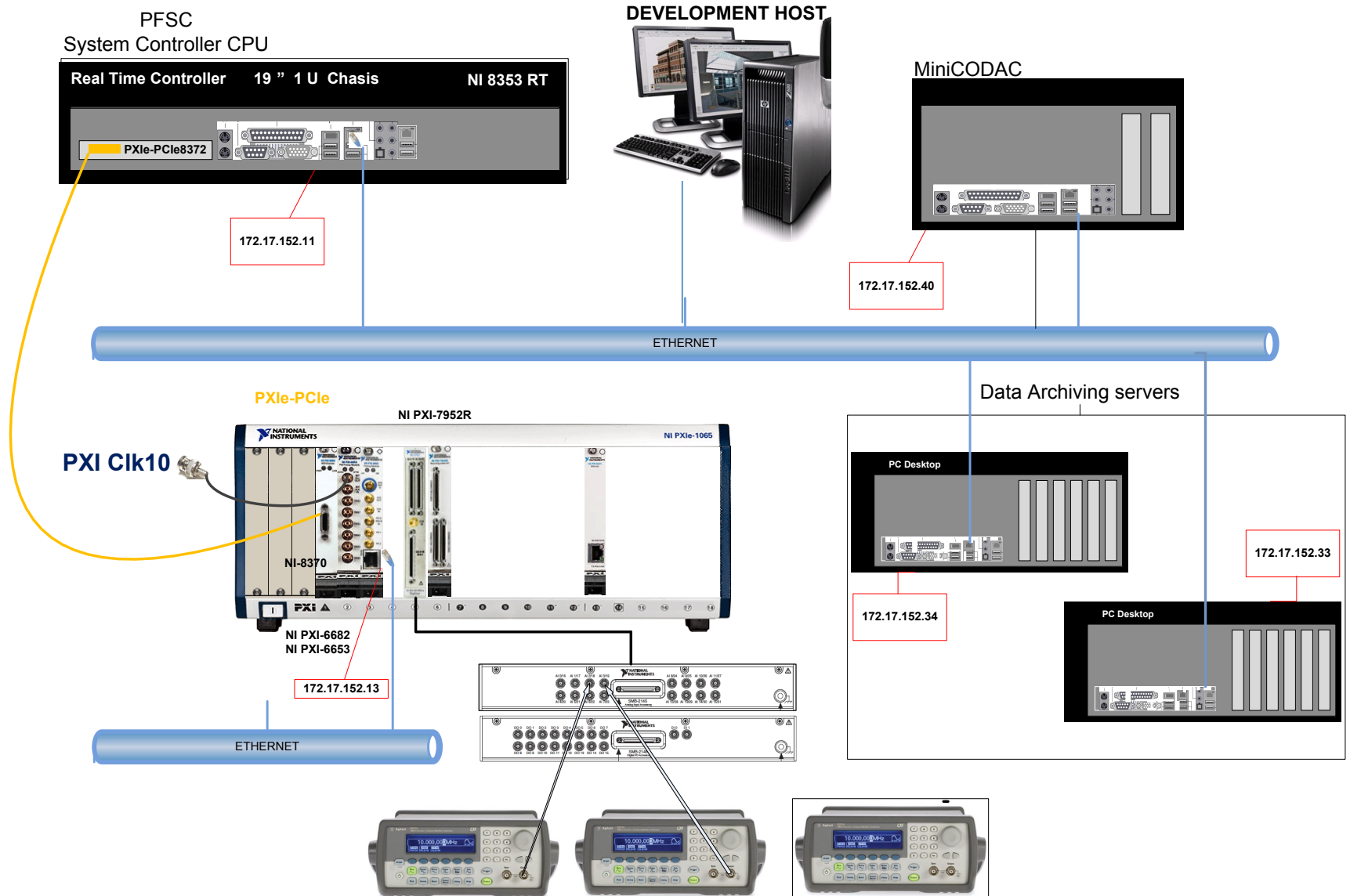


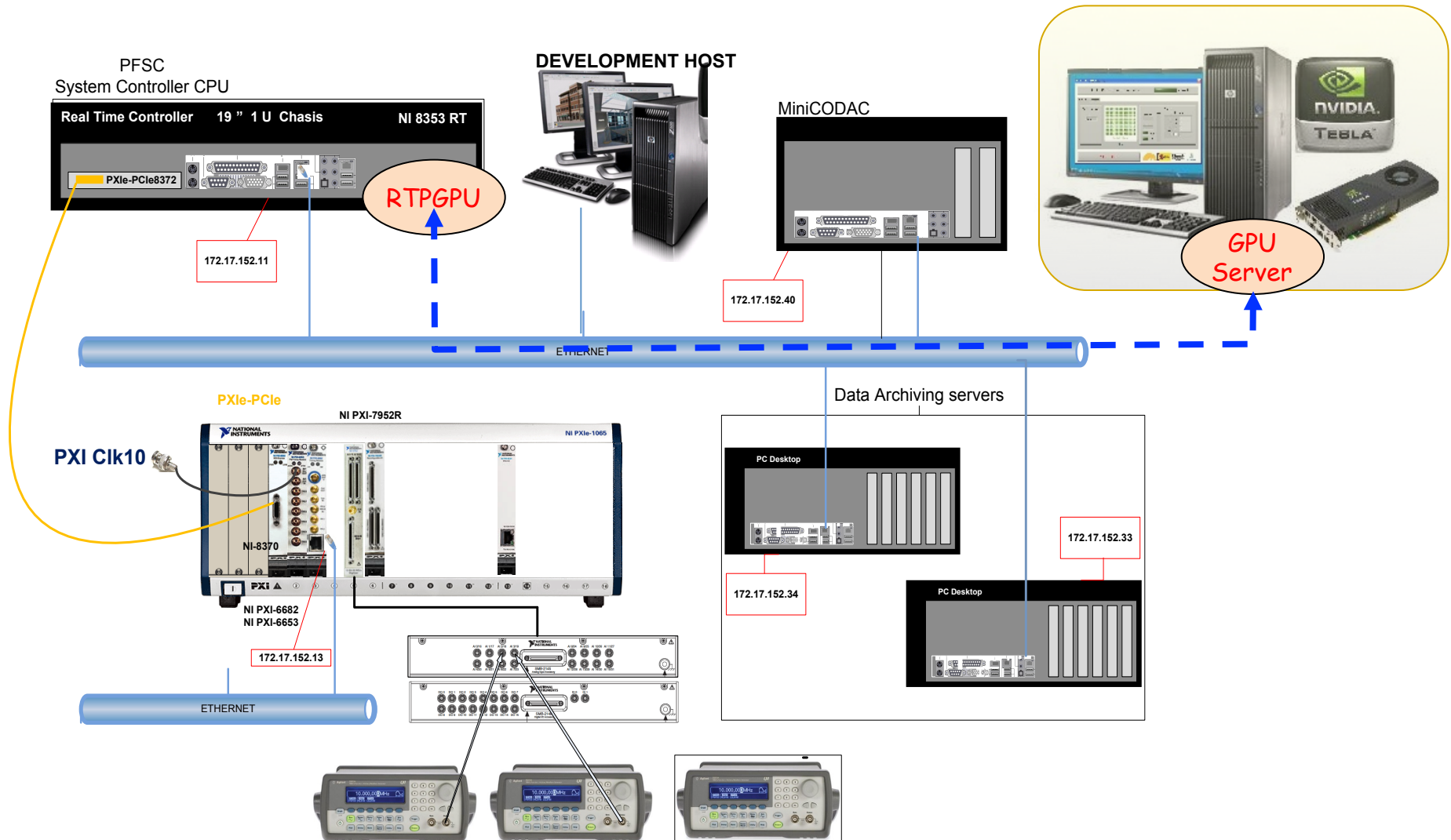
# ATCA form factor (IST/IPFN): Alpha version



- Requirements
  - Hardware: COTS
  - Software: Linux RHEL 64 bits & EPICS
- Issues (2010)
  - The drivers (and device support ) are not available under Linux 64 bits
    - Other people in charge of the development
    - Greatly complicated development to be finished in a limited time
- Solution for alpha version:
  - Labview Real Time based (to avoid third parties dependences, to test system capabilities and to learn about problems and gain experience for the beta version)
  - PXIe solution using:
    - National Instruments hardware (PXI chassis, timing modules, DAQ using FlexRIO and external controller)
    - LabVIEW RT Module applications running in the controller
    - LabVIEW FPGA for FlexRIO
    - LabVIEW EPICS IOC for real time target for supporting channel access.
    - Specific application developed running in external computers for streaming/archiving, data processing with GPUs, and monitoring using ITER CODAC Core System.

# HW elements: Block Diagram







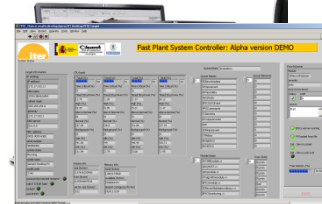
# Development tools

PFSC  
System Controller CPU

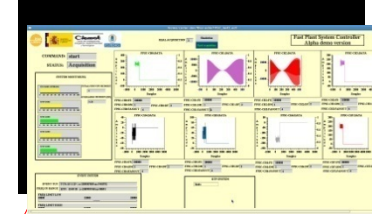


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DEVELOPMENT HOST



MiniCODAC



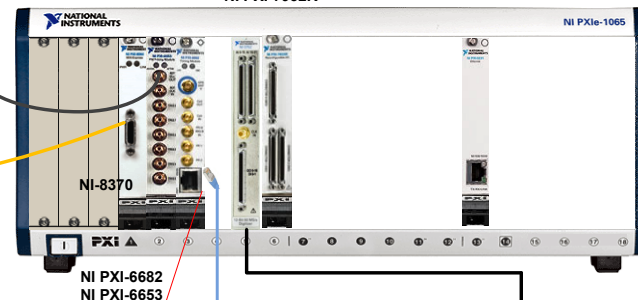
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ETHERNET

PXIe-PCle

NI PXI-7952R

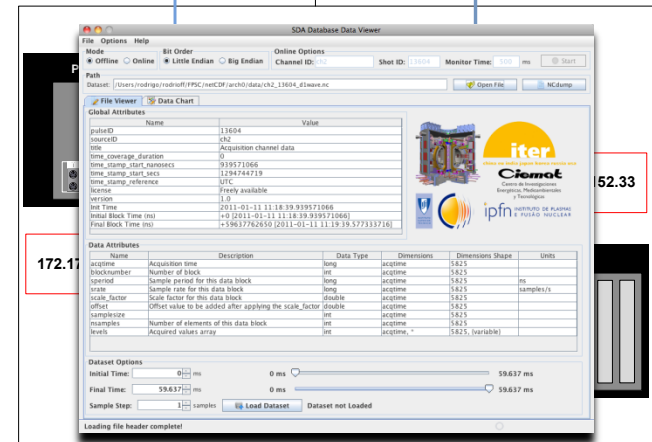
PXI Ck10



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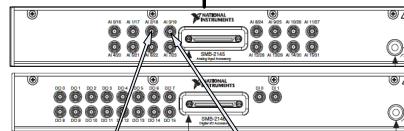
ETHERNET

Data Archiving servers



52.33

172.17





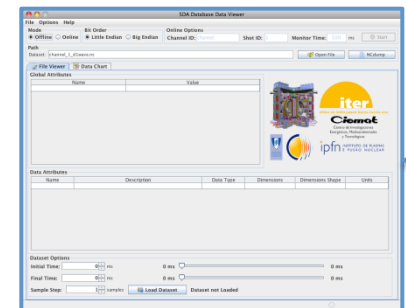
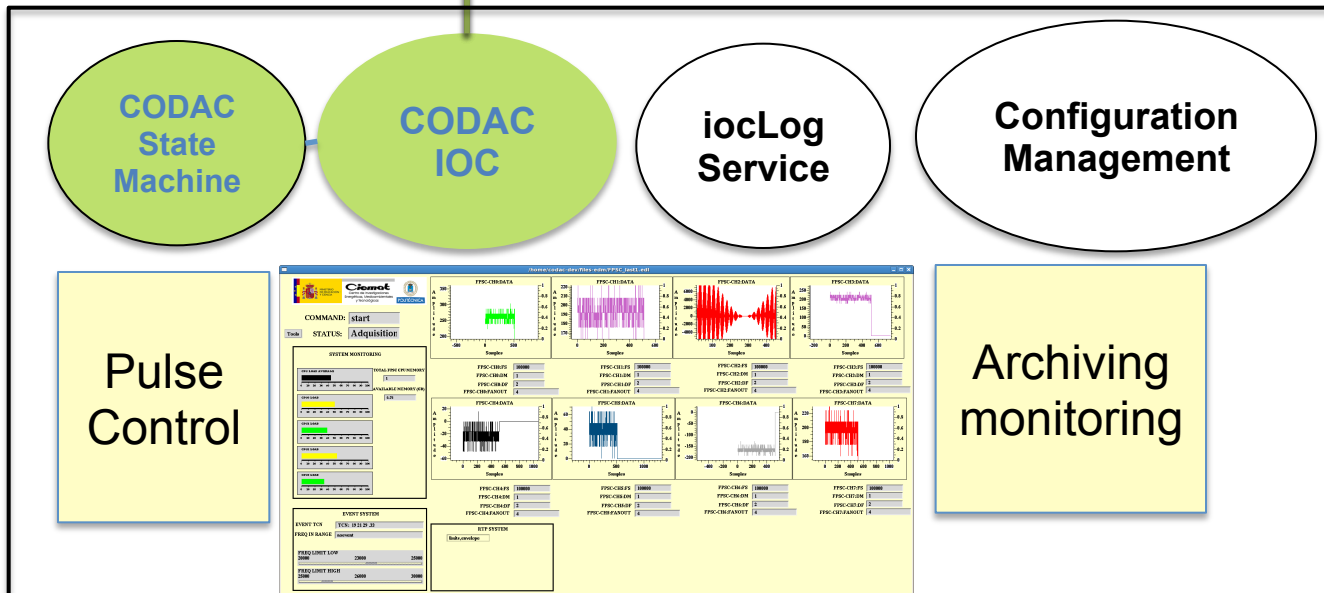
# FPSC software elements



Development System



Signal Generator



Archive Viewer

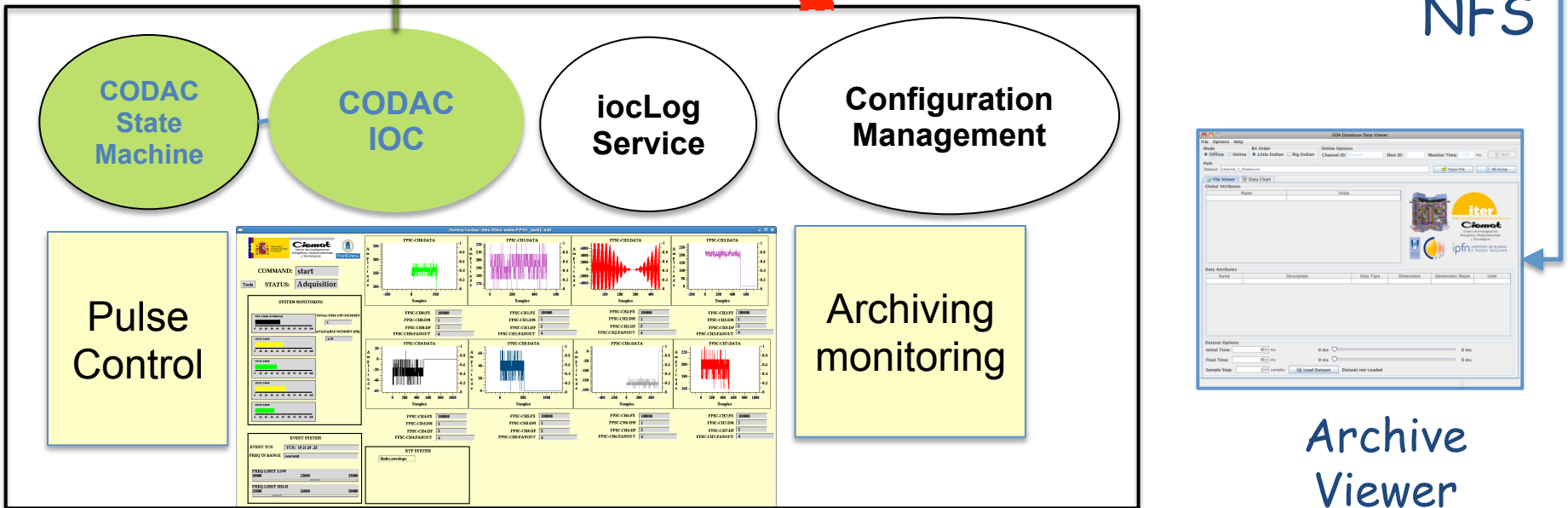
## FPSC software elements



## Development System



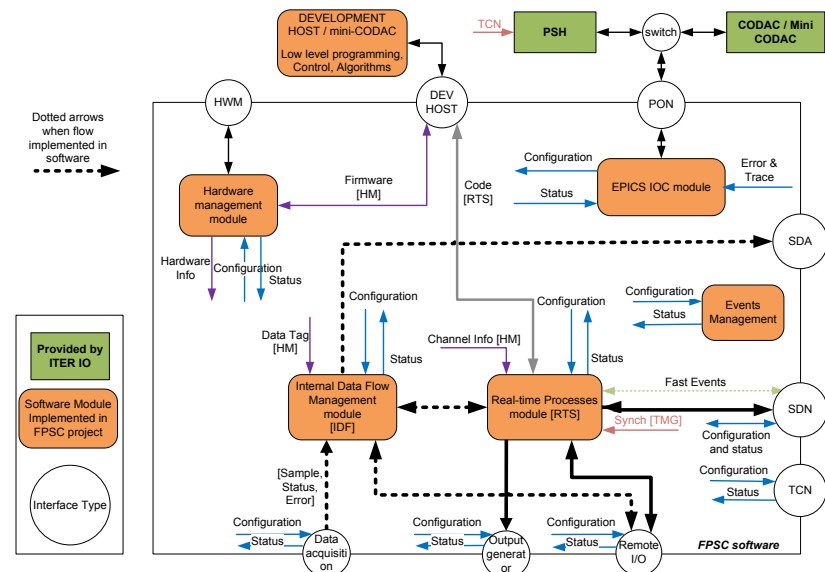
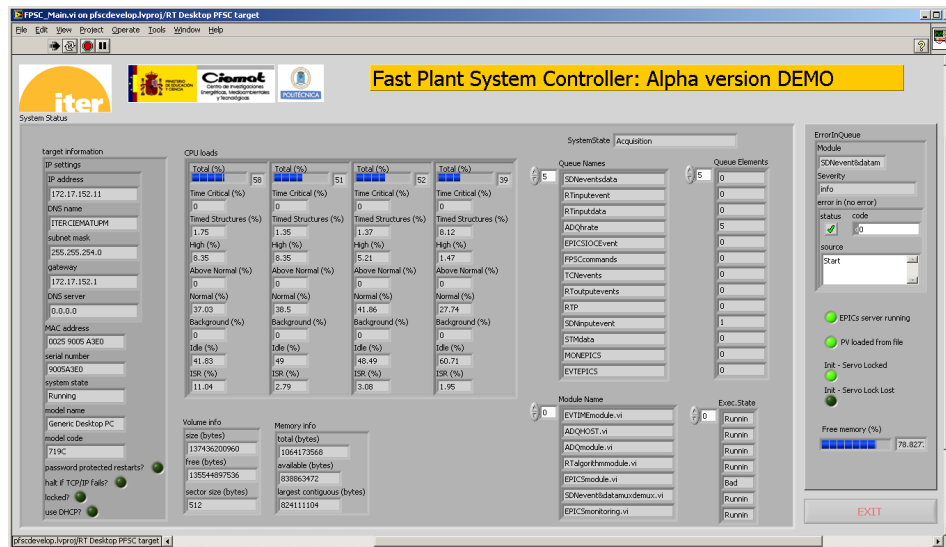
## Signal Generator



# FPSC applications running in NI8353 computer

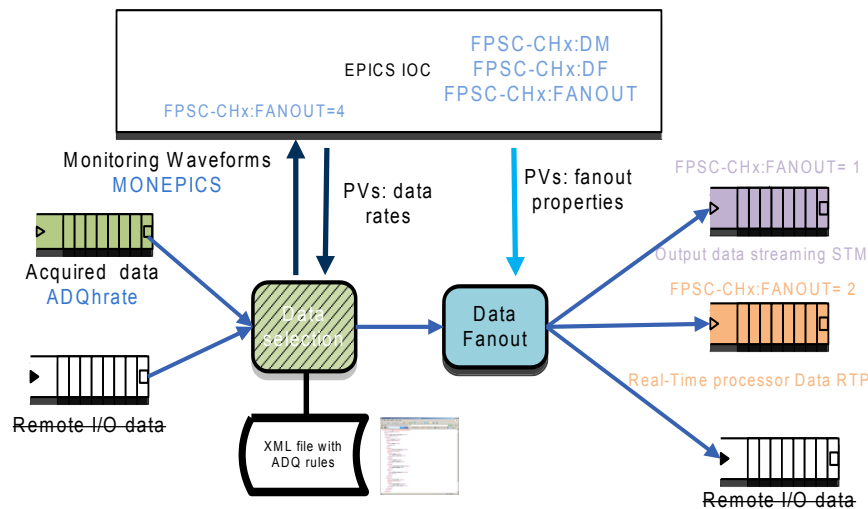
## • LabVIEW Modules implemented:

- **CORE**. General queues management. Creation, destruction and state machine control.
- **EPICS-IOC**. Channel access and PVs management.
- **TCN**. Management of PXI6653 and PXI6682 for clock generation and event time-stamping.
  - PXI CLK 10MHz is in phase with PXI6682 IEEE1588 clock
- **ACQ**. Data acquisition and selection.
- **FPGADAC**. Data acquisition application for RIO devices with time-stamping. Also include a signal simulator (inside FPGA) for debugging purposes.
- **EVT**. Event management. **SDN**. Implemented using NI-Time Triggered Variables
- **RTP**. Real time processing. Basic algorithms. **RTPGPU**. GPU management.



# Main features of FPSC software

- ADQ parameters are controlled & changed using PVs (also during the pulse):
  - Sampling rate and block size for FlexRIO device.
  - Decimation factor and modes (samples and blocks) for EPICS monitoring
- FPSC State machine control and status using PVs: start/stop, memory used, CPU load, etc.
- Acquired data can be sent to streaming, monitoring with EPICS, real time processing and GPU using «FANOUT PVs».
- Preprocessing algorithms can be dynamically selected using PVs.



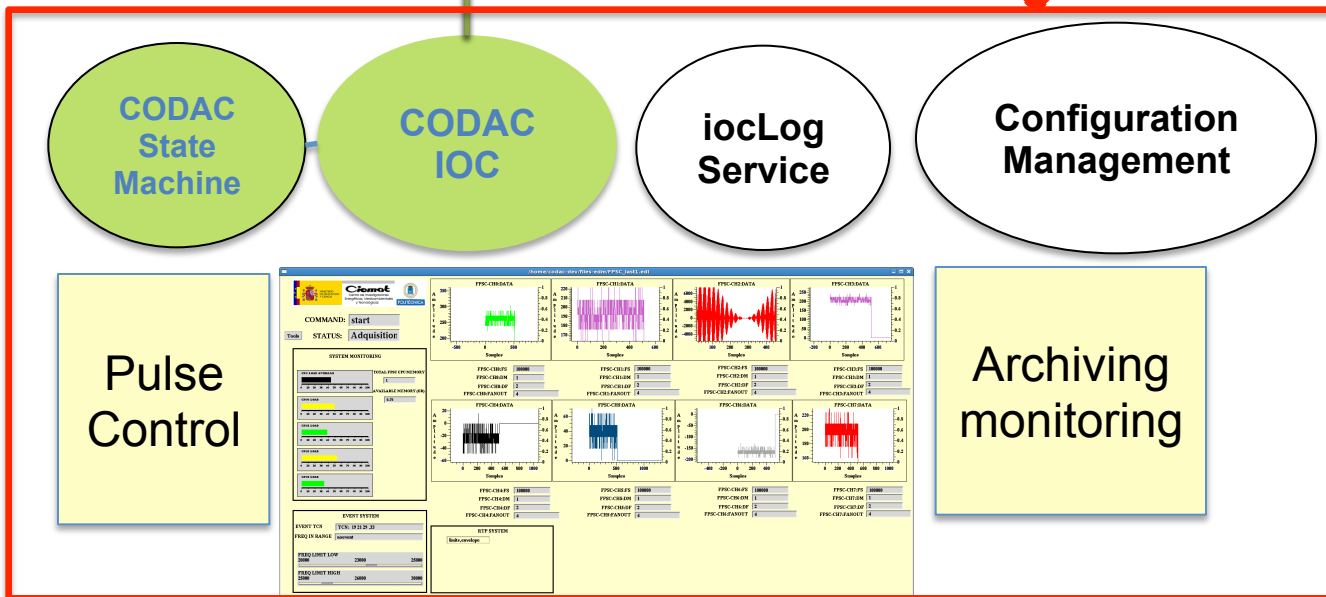
# FPSC software elements



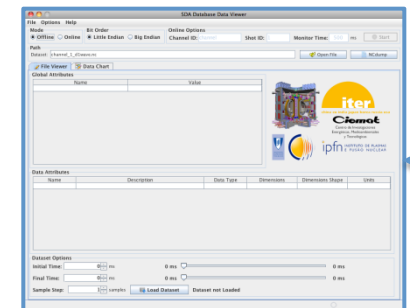
Development System



Signal Generator



NFS

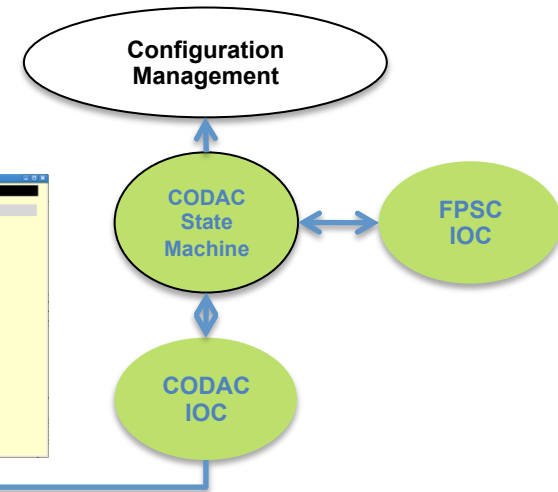


Archive Viewer

The screenshot displays the 'Fast Plant System Controller Alpha demo version' interface. At the top, the URL 'http://192.168.1.100:8080/FFC\_Soft\_v01' is shown. The interface is divided into several functional areas:

- COMMAND:** Includes buttons for 'start' and 'Acquisition'.
- SYSTEM MONITORING:** Contains a 'CPU usage' section with a bar chart and a 'I/O' section with a table of data. Below these are several small plots showing system performance metrics.
- RSP SYSTEM:** A large plot area at the bottom right, currently blank, with a 'Data' label.

The main display area features 18 subplots arranged in a 3x6 grid. Each subplot shows a different data series over time, with labels such as 'FFC-CRDATA' and 'FFC-CRDATA'.



```
File Edit View Terminal Tools Help
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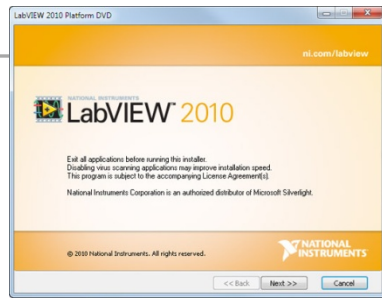
```
root@localhost:~# cd /opt/codas-3.0/examples/mc-sample-mcr/main/epics && ./test -x test -v 17:15:18.968870 Tue Jan 15 17:17:18 2013 sevr: info module: RTapiRTModule.vi -- Start  
17:15:18.968870 Tue Jan 15 17:17:18 2013 sevr: info module: FPG STN Module.vi -- Start  
17:15:18.968870 Tue Jan 15 17:17:18 2013 sevr: info module: ADGOST.vi -- Start  
localhost.localdomain:3752 Tue Jan 15 17:17:18 2013 sevr+info Putting  
17:15:18.968870 Tue Jan 15 17:18:18 2013 sevr: info module: FPGAExtModules.vi -- Start  
17:15:18.96952 Tue Jan 15 17:18:18 2013 sevr: info module: EXTIRModule.vi -- Stop  
sevr: info module: ADGOST.vi -- Stop  
17:15:18.96952 Tue Jan 15 17:18:18 2013 sevr: major module: ARDmodule.vi -- Dequeue Element in ARDmodule.vi--FPGA_Main.vi code: 1122  
17:15:18.96952 Tue Jan 15 17:18:18 2013 sevr: info module: RTapiRTModule.vi -- Stop  
17:15:18.96952 Tue Jan 15 17:18:18 2013 sevr: info module: SIBServerLocalcomms.vi -- Stop  
17:15:18.96952 Tue Jan 15 17:18:18 2013 sevr: info module: EPICScoring.vi -- Stop  
17:15:18.96952 Tue Jan 15 17:18:18 2013 sevr: info module: EPICSControl.vi -- Dequeue Element in FPSC STN Module.vi--FPSC_Main.vi code: 1122  
17:15:18.96963 Tue Jan 15 17:18:18 2013 sevr: major module: FPGC STN Module.vi -- Dequeue Element in FPGC STN Module.vi--FPGA_Main.vi code: 1122  
sevr: info module: FPGC STN Module.vi -- Dequeue Element in FPGC STN Module.vi--FPGA_Main.vi code: 1122  
17:15:18.96963 Tue Jan 15 17:18:18 2013 sevr: info module: FPGC STN Module.vi -- Stop  
sevr: info module: FPGC STN Module.vi -- Acquisition State End  
localhost.localdomain:3752 Tue Jan 15 17:18:18 2013 sevr+info Putting State AfterPutschance  
17:15:18.96963 Tue Jan 15 17:18:18 2013 sevr: info module: TCM_WebEvent.vi -- Stop  
17:15:18.96970 Tue Jan 15 17:18:18 2013 sevr: info module: FPGC_Main.vi -- Acquistion State End  
17:15:18.96968 Tue Jan 15 17:18:18 2013 sevr: info module: FPGC_Main.vi -- Error State  
17:15:18.96970 Tue Jan 15 17:18:21 2013 sevr: info module: FPGC_Main.vi -- Idle State
```

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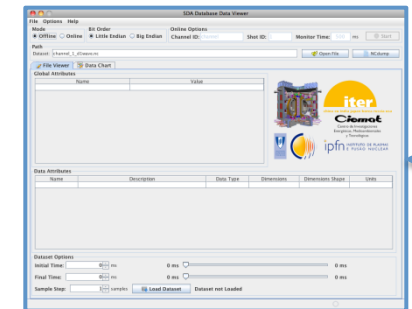
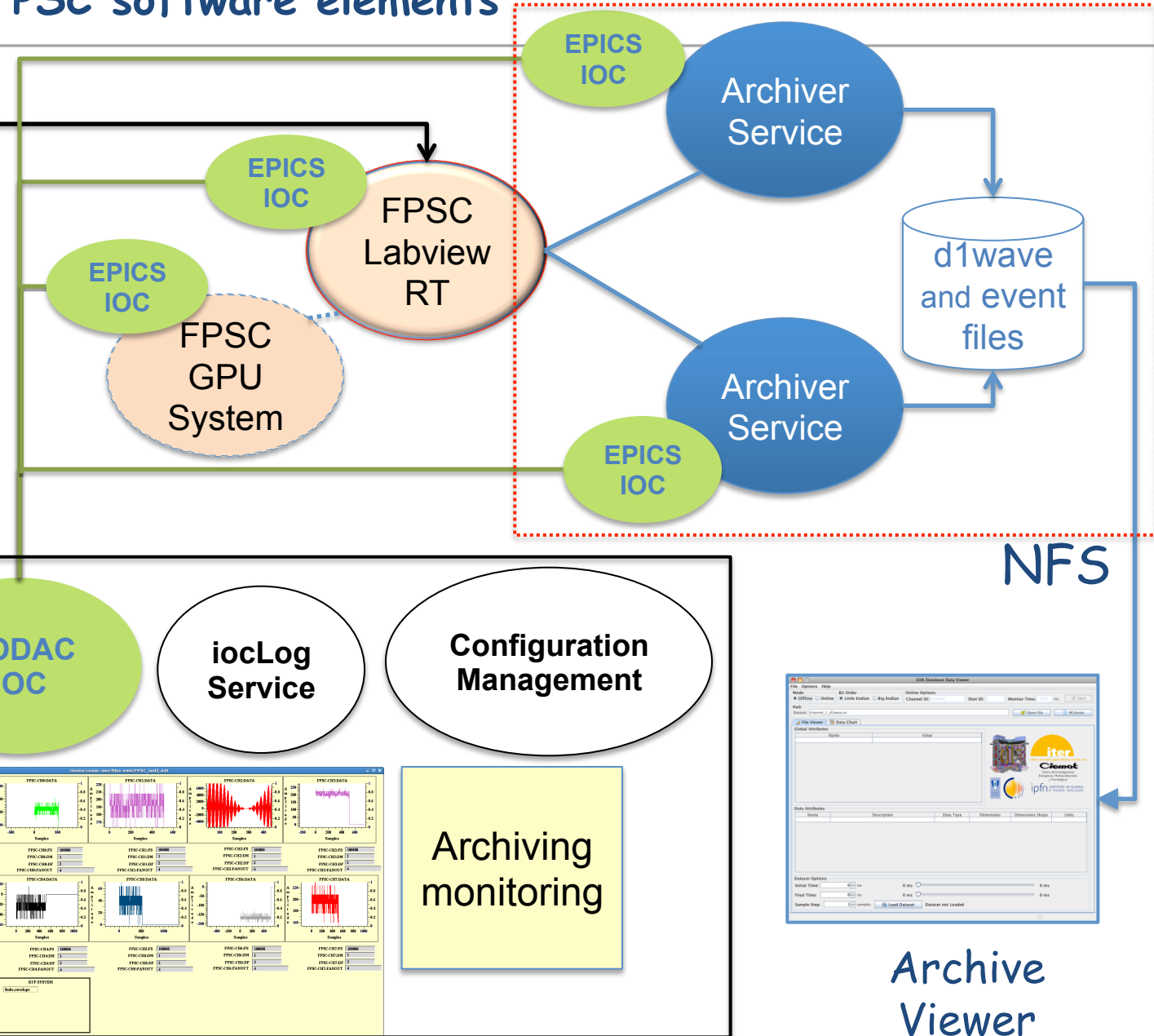
# FPSC software elements



Development System



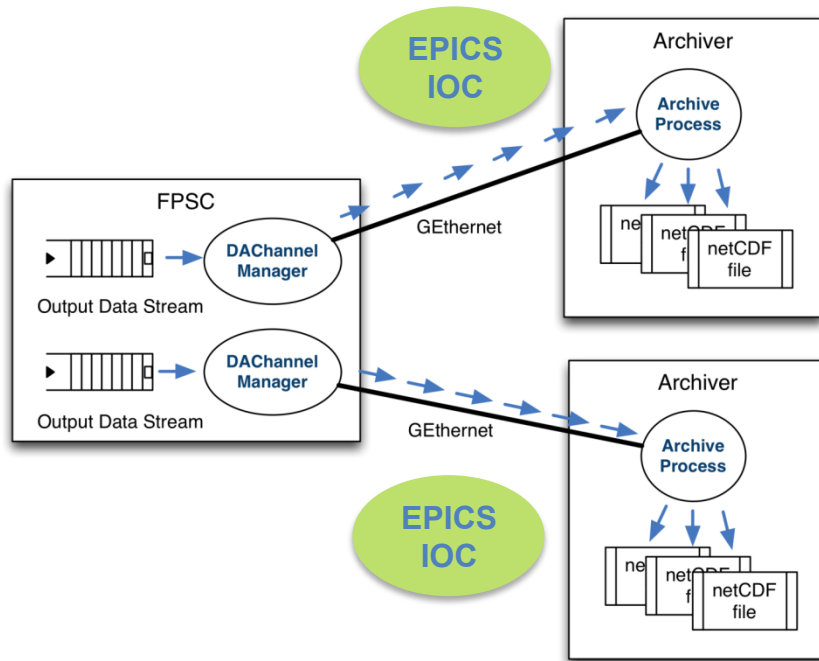
Signal Generator



Archive Viewer



# Archiving System



- Data sources can be assigned to data archivers
- netCDF file is the fundamental storage unit
- A file per data source (signal) and pulse
- Two types of data are currently implemented: "d1wave" and "event".
- EPICS IOC currently used for monitoring

# Archiving Viewer and monitoring

**Global Attributes**

Name	Value
pulseID	13604
sourceID	ch2
title	Acquisition channel data
time_coverage_duration	0
time_stamp_start_nanosecs	939571066
time_stamp_start_secs	1294744719
time_stamp_reference	UTC
license	Freely available
version	1.0
Init Time	2011-01-11 11:18:39.939571066
Initial Block Time (ns)	+0 [2011-01-11 11:18:39.939571066]
Final Block Time (ns)	+59637762650 [2011-01-11 11:19:39.57733716]

**Data Attributes**

Name	Description	Data Type	Dimensions	Dimensions Shape	Units
acqtime	Acquisition time	long	acqtime	5825	
blocknumber	Number of block	int	acqtime	5825	
speriod	Sample period for this data block	long	acqtime	5825	ns
srate	Sample rate for this data block	long	acqtime	5825	samples/s
scale_factor	Scale factor for this data block	double	acqtime	5825	
offset	Offset value to be added after applying the scale_factor	double	acqtime	5825	
samplesize		int	acqtime	5825	
nsamples	Number of elements of this data block	int	acqtime	5825	
levels	Acquired values array	int	acqtime, *	5825, (variable)	

**Dataset Options**

Initial Time: 0 ms      0 ms      59.637 ms

Final Time: 59.637 ms      0 ms      59.637 ms

Sample Step: 1 samples      **Load Dataset**      Dataset not Loaded

Loading file header complete!

- "Online" and "Offline" mode
- On remote via NFS (Network File System)
- Time slice positioning
- Self Description data visualization
- Flexible plotter
  - Zooms
  - Export options
- Completely based on EPICS channel access
  - Every archiver implements its own EPICS IOC
- System variables:
  - CPU load
  - Memory Usage
- Archiving system performance
  - Receiving data rate per channel
  - Total received data rate
  - Storing data rate per channel
  - Total saved data rate

# Conclusions

- Implementation of a basic FPSC devoted to data acquisition following essential ITER requirements:
  - “Intelligent data acquisition” using FPGA DAQ devices with IEEE-1588 time-stamping.
  - System DAQ parameters controlled by EPICS’ PVs (**changed dynamically during the PULSE**)
  - Streaming capabilities.
  - Preprocessing algorithms using local processor and GPU (**controlled with EPICS PVs**).
  - Integration with EPICS CODAC system (v1.1).
  - **100kS/s per channel with streaming, time-stamping, EPICS monitoring, and 2 channels preprocessing**
- LabVIEW based tools (RT/FPGA) have been a good choice for quick prototyping in a **short period** of time (3 months).
  - Graphical oriented design simplifies: the definition of complex software models , the debugging of the different applications, and the test of complex hardware setups.

# ITER Fast Plant System Controller Prototype Based on PXI Platform

Thank you for your attention!!

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Thank you to NI for the strong support in the development of this  
project